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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,325	01/09/2004	Masayuki Furumiya	Q79080	7256

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/753,325	FURUMIYA ET AL.
	Examiner	Art Unit
	Steven Loke	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/9/04, 9/21/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 7-8, the phrase "said first electrode and said first electrode of the wiring layer" is unclear whether it is being referred to "said first electrode of one wiring layer and said first electrode of an adjacent wiring layer"; line 9, the phrase "its upper layer or lower layer" is unclear whether it is being referred to a wiring layer formed above or below the one wiring layer"; lines 10-11, the phrase "said second electrode and said second electrode of the wiring layer" is unclear whether it is being referred to "said second electrode of one wiring layer and said second electrode of an adjacent wiring layer"; line 12, the phrase "its upper layer or lower layer" is unclear whether it is being referred to a wiring layer formed above or below the one wiring layer.

Claim 2, lines 2-3, the phrase "a same design rule" is unclear as to what design rule is it being referred to.

Claim 7, lines 3-4, claim 8, lines 4-5, the phrase "the minimum value that is allowed by the design rule of said wiring layer" is unclear as to what minimum value and what design rule is it being referred to.

Claim 11, lines 2-4, the phrase "the minimum value allowed by the design rule of said wiring layers" is unclear as to what minimum value and what design rule is it being referred to.

Claim 17, lines 4-5, the phrase "said capacitor is a decoupling capacitor connected to a power source in parallel" is unclear as to how a capacitor connected to a power source in parallel.

Claim 20, line 9, the phrase "the electrodes" is unclear whether it is being referred to "the first and second electrodes"; lines 11-12, the phrase "one terminal out of said first and second terminals" is unclear whether it is being referred to another terminal different from the one of the first and second terminals that connected to the higher potential.

Claim 21, line 11, the phrase "the electrodes" is unclear whether it is being referred to "the first and second electrodes"; lines 13-14, the phrase "one terminal out of said first and second terminals" is unclear whether it is being referred to another terminal different from the one of the first and second terminals that connected to the higher potential.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 9, 12 and 13 insofar, as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sowlati et al. (in the IDS filed on 9/21/04).

In regards to claim 1, Sowlati et al. show all the elements of the claimed invention in figs. 2A-2C. It is a semiconductor device, comprising: a plurality of wiring layers [22-25]

that are laminated with each other, each of said wiring layers includes: an interlayer insulating film [26-29, 34]; first and second electrodes [22-25] buried in the interlayer insulating film and remote from each other; a first via ([30-32] in layers B) that connects said first electrode of one wiring layer and said first electrode of an adjacent wiring layer, which is provided on a wiring layer above or below the one wiring layer, to each other; and a second via ([30-32] in layers A) that connects said second electrode of one wiring layer and said second electrode of an adjacent wiring layer, which is provided on a wiring layer above or below the one wiring layer, to each other, and said first electrode and said first via are connected to a first terminal B, said second electrode and said second via are connected to a second terminal A, and a capacitor is formed between said first electrode and said first via, and said second electrode and said second via.

In regards to claim 2, Sowlati et al. further disclose a plurality of said wiring layers are provided in a same design rule (length and width) with each other.

In regards to claim 3, Sowlati et al. further disclose said wiring layers [22-25] are provided in three or more layers.

In regards to claim 4, Sowlati et al. further disclose a plurality of said first via ([30-32] in layers B) are arranged in a position where the via overlap with each other and a plurality of said second via ([30-32] in layer A) are arranged in a position where the via overlap with each other, viewing from the lamination direction of said wiring layers.

In regards to claim 5, Sowlati et al. further disclose a plurality of said first electrodes ([22-25] in layers B) are arranged in a position where the electrodes overlap with each other and a plurality of said second electrodes ([22-25] in layers A) are arranged in a

position where the electrodes overlap with each other, viewing from the lamination direction of said wiring layers.

In regards to claim 9, Sowlati et al. further disclose said first and second electrodes are in strip shapes that are parallel to each other.

In regards to claim 12, Sowlati et al. further disclose said first and second electrodes are provided in each of said wiring layers in plural numbers, and said first and second electrodes are arrayed alternately in each wiring layer.

In regards to claim 13, Sowlati et al. further disclose regarding each of said first and second electrodes, said first and second via are provided in plural numbers by being arrayed in the longitudinal direction of said first and second electrodes (fig. 2B).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-8, 10, 11, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sowlati et al. in view of Hajimiri et al. (in the IDS filed on 9/21/04).

In regards to claims 6, 10, Sowlati et al. differ from the claimed invention by not showing the distance between said first and said second electrode is 0.3 μm or less in a same wiring layer.

Hajimiri et al. disclose the distance (L_{min}) between said first and said second electrode is 0.1 μm or less in a same wiring layer (col. 9, line 44) in a vertical parallel plate capacitor.

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the distance of Hajimiri et al. in Sowlati et al. because more capacitors can be formed in an integrated circuit.

In regards to claims 7, 11, Sowlati et al. differ from the claimed invention by not showing the distance between said first electrode and said second electrode in a same wiring layer is the minimum value that is allowed by the design rule of said wiring layer.

Hajimiri et al. disclose the distance (L_{min}) between said first and said second electrode in a same wiring layer is the minimum value that is allowed by the design rule of said wiring layer in a vertical parallel plate capacitor (col. 9, line 44 and fig. 11).

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the distance of Hajimiri et al. in Sowlati et al. because more capacitors can be formed in an integrated circuit.

In regards to claim 8, Sowlati et al. differ from the claimed invention by not showing the distance between said first via and said second via that is formed in the closest position to the first via is the minimum value that is allowed by the design rule of said wiring layer.

Hajimiri et al. disclose the distance (L_{min}) between said first and said second electrode in a same wiring layer is the minimum value that is allowed by the design rule of said wiring layer in a vertical parallel plate capacitor (col. 9, line 44 and fig. 11). Therefore, the distance between said first via and said second via that is formed in the closest position to the first via is the minimum value that is allowed by the design rule of said wiring layer.

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the distance (the distance between the first and second via) of Hajimiri et al. in Sowlati et al. because more capacitors can be formed in an integrated circuit.

In regards to claim 14, Sowlati et al. differ from the claimed invention by not showing the distance between said first via in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers.

Hajimiri et al. show the distance between said first via [304] in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers in fig. 5.

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the via arrangement of Hajimiri et al. in Sowlati et al. because they reduce the series resistance of the capacitor.

In regards to claim 15, Sowlati et al. differ from the claimed invention by not showing at least one of said first and second via is a slit-shaped via extending in the longitudinal direction of said first and second electrodes.

Hajimiri et al. show at least one of said first and second via [304] is a slit-shaped via extending in the longitudinal direction of said first and second electrodes [306] in fig. 3.

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the slit-shaped via of Hajimiri et al. in Sowlati et al. because it increases the quality factor for a given capacitor value.

7. Claims 16-21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: The first major difference in the claims not found in the prior art of record is the diameter of said first and second via are larger than the diameter of the via provided in an integrated circuit section. The second major difference in the claims not found in the prior art of record is said first terminal is connected to ground wiring and said second terminal is connected to power source wiring. The third major difference in the claims not found in the prior art of record is another capacitor with upper and lower electrodes formed under the capacitor with via and connected to first and second terminals. The fourth major difference in the claims not found in the prior art of record is another capacitor with N-type semiconductor layer and P-type semiconductor layer formed under the capacitor with via and connected to first and second terminals.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
March 19, 2005

Steven Loke